REMARKS

Claims 1-11 were examined. All claims were rejected. In response to the above-identified Office Action, Applicant amends claims 1-4 and 7-9 and adds new claim 12, but does not cancel any claims. Reconsideration of the rejected claims in light of the aforementioned amendments and the following remarks is requested.

I. Claims Rejected Under 35 U.S.C. § 112, Second Paragraph

The Examiner rejected claims 9 and 10 under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter Applicant regards as the invention. In this Response, Applicant amends claim 9 to correct an antecedent error noted by the Examiner. Claim 10, which depends upon claim 9, also benefits from this correction. It is believed that the amendment fully addresses this ground of rejection, so the Examiner is respectfully requested to withdraw the rejection.

II. Claims Rejected Under 35 U.S.C. § 102(b)

The Examiner rejected claims 1, 2 and 11 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,902,910 issued to Hsieh ("*Hsieh*"). Although there are some similarities between *Hsieh*'s circuit at Fig. 8 and the claimed power-up circuit, a close examination of the claim elements shows that Applicant's invention is different, and not taught or suggested by the references of record.

First, claim 1 recites that the power supply voltage level follower unit provides a bias voltage which is linearly varied according to variation of a power supply voltage. (*See* eq. 1 on p. 4 and lines 20-23 on p. 7.) The structure in *Hsieh* that allegedly reads on this follower unit, element 4-1A of Fig. 8, is actually an inverter whose trigger point is determined by the sizes of the MOS transistors P4A, P5A and N7A'. The inverter has a *non-linear* transfer function, as can be seen in *Hsieh*'s Fig. 9 graph of $V_{4A'}$. Therefore, element 4-1A is different from the claimed level follower.

Second, claim 1 recites generating a power-up signal by performing a pull-down operation controlled by the detection signal and a delayed detection signal to thereby prevent a logic level of the power-up signal from transitioning during a power drop of the power supply voltage. In *Hsieh*, the structure that allegedly corresponds to the

claimed reset prevention unit is an ordinary logic gate (Fig. 8, element 83) and not a circuit to perform a pull-down operation.

For at least these reasons, Applicant believes that *Hsieh* fails to teach every element of the claimed power-up circuit, and respectfully requests that the Examiner withdraw the rejection of claim 1.

As to claims 2 and 11, those claims depend directly or indirectly upon claim 1, and are patentable for at least the reasons discussed in support of that base claim. Applicant requests that the Examiner withdraw the rejections of claims 2 and 11 as well.

III. Claims Rejected Under 35 U.S.C. § 103(a)

The Examiner rejected claims 3-10 under 35 U.S.C. § 103(a) as unpatentable over *Hsieh* (*supra*) in view of U.S. Patent No. 5,889,416 issued to Lovett ("*Lovett*"). Each of the rejected claims depends directly or indirectly upon claim 1, which was discussed in the preceding section. *Lovett* is relied upon for its teaching of "an improved NAND gate having the benefit of uniform slew rate," and Applicant has been unable to locate any portion of *Lovett* that concerns a power-up circuit, or teaches or suggests a power supply voltage level follower for providing a bias voltage which is linearly varied according to variation of a power supply voltage. Therefore, claims 3-10 are allowable for at least the reasons discussed in support of their base claim. The Examiner is respectfully requested to withdraw the rejections of these claims.

IV. New Claim

Applicant has added new claim 12 to particularly point out and distinctly claim material that is regarded as the invention. The claim is supported by the specification at, *e.g.*, p. 6, lines 9-11; p. 9, lines 2-7; and Fig. 3. In particular, claim 12 includes the power supply voltage level follower unit to provide a bias voltage which varies linearly with a power supply voltage, a feature noted to be absent from *Hsieh* and *Lovett*. Thus, the new claim is believed to be allowable over the references of record.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-12, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

Dated: 5/10, 2005

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

Eric S. Hyman, Reg. No. 30,139

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025

(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that the correspondence is being deposited with the United States Postal Service, with sufficient postage, as first class mail in an envelope addressed to:

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Marilyn Bass 05-10-05

Marilyn Bass Date